

Claim Amendments

1 1. (currently amended) An apparatus for adding a plurality of partial
2 products ~~output~~ comprising:

3 a plurality of carry-save adders coupled together in series, each of the
4 carry-save adders in the series receiving one of the plurality of partial products
5 and two intermediate vectors from a prior carry-save adder in the series of carry-
6 save adders, and outputting a carry bit, a sum bit and two intermediate vectors,
7 wherein the first one in the series of carry-save adders receives two of the
8 plurality of partial products;

9 a last carry-save adder coupled to a last one in the series of carry-save
10 adders and receiving a last partial product of the plurality of partial products and
11 two intermediate vectors from a last one in the series of carry-save adders, and
12 outputting a carry vector (Cmsb) and a sum vector (Smsb);

13 a plurality of carry-propagate adders coupled in series and coupled to the
14 plurality of carry-save adders, each of said plurality of carry-propagate adders
15 outputting a resulting bit and a carry bit; and

16 an output register coupled to the first one in the series of carry-save
17 adders, the last carry-save adder, and the plurality of carry-propagate adders, and
18 storing the plurality of resulting bits, the sum bit output by the first one in the
19 series of carry-save adders and the carry bit output by the last one in the series of
20 carry-propagate adders.

1 2. (currently amended) The apparatus according to claim 1, further
2 comprising:

3 an a MOST SIGNIFICANT BIT carry output register coupled to the last
4 carry-save adder and storing the most significant bit carry vector (Cmsb); and

5 a MOST SIGNIFICANT BIT sum output register coupled to the last
6 carry-save adder and storing the most significant bit sum vector (Smsb)

1 3. (original) The apparatus according to claim 1, wherein at least one of
2 the carry-propagate adders comprises a half-adder and the other carry-propagate
3 adders comprise full-adders.

1 4. (original) An apparatus for adding a plurality of partial products
2 comprising:

3 a plurality of carry-save adders coupled together in series, each of the
4 plurality of carry-save adders receiving a successive one of the plurality of partial
5 products and two intermediate vectors (In-1, In-2) from a prior carry-save adder
6 in the series of carry-save adders and each of the plurality of carry-save adders
7 outputting a carry bit (Cn-1) a sum bit (Sn-1) and two intermediate vectors (In,
8 In+1) wherein a first one in the series of carry-save adders receives two of the
9 plurality of partial products;

10 a last carry-save adder coupled to a last one in the series of carry-save
11 adders, receiving a last one of the plurality of partial products and two
12 intermediate vectors from said last one in the series of carry-save adders, and
13 outputting a plurality of sum bits and a plurality of carry bits; and

14 a plurality of half-adder/full-adder series combinations coupled to the last
15 carry-save adder, each of the plurality of half-adder/full-adder series combinations
16 receiving two carry bits of the plurality of carry bits output by the last carry-save
17 adder and two sum bits of the plurality of sum bits output by the last carry-save
18 adder, and outputting two result bits and a carry bit.

1 4. 5. (currently amended) The apparatus according to ~~claim 3~~ claim 4,
2 further comprising:

3 two half-adders coupled together in series and coupled to the last carry-
4 save adder, said two half-adders receiving from the last carry-save adder two most
5 significant carry bits and a most significant sum bit and outputting two result bits

6 and a carry bit as a plurality of most significant bits of the result of adding the
7 plurality of partial products.

1 5. 6. (currently amended) The apparatus according to ~~claim 4~~ claim 5,
2 further comprising a single output register coupled to the plurality of half-
3 adder/full-adder combinations and storing the two result bits and the carry bit
4 output by each of the plurality of half-adder/full-adder series combinations.

1 7. (New) A method of reducing the speed of a multiplier comprising the
2 step of:
3 replacing carry and save registers [49a, 49b] relating to a set of least significant
4 bits with a single register [48] and a carry-propagate adder comprising a half adder [37]
5 and a set of full adders [38-40].

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